ISL6405 Dual LNB Controller with I^{2}C Interface for Advanced Satellite Set-Top Box Designs

PRELIMINARY

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Introduction

Communication Satellite Frequency Allocation

Communication satellites operate within two frequency bands for TV/Broadband service broadcast signals, C Band and Ku Band. The C Band overall frequency spectrum is 4.0GHz - 8.0GHz, while the Ku Band overall frequency spectrum is 11.7GHz -18.0GHz.

Within these bands each satellite will have specific uplink and downlink frequency allocation. For example the North American DBS system has categories assigned as follows, Ku Band high power downlink is 12.2GHz –12.7GHz and 17.3GHz-17.8GHz as the uplink frequency, C Band downlink frequency is 3.7GHz to 4.2GHz and 5.925GHz-6.425GHz as uplink frequency.

Also, to use the frequencies that are available for satellite broadcast as efficiently as possible, and to accommodate additional number of channels within a given frequency band, the transmission signal can be formatted to be either vertical and horizontal, or circular right-hand and circular left-hand simultaneously per frequency.

What is a Low Noise Block (LNB)?

An LNB is a low noise block module, placed on the focus of the dish antenna (parabola) that provides the following functions:

- Down conversion of the incoming the signal from GHz range to 910MHz -2150MHz (for Europe) range called “first conversion signal.” This conversion allows the signal to be carried by an inexpensive co-axial cable towards the receiver.
- Signal amplification with good noise factor. The LNB improves the first conversion signal level through the use of a built-in low noise amplifier.
- Selects Vertical or Horizontal polarization.
- Selects operating band by switching its internal oscillator from Low band to High band when it “receives” a 22kHz tone. Specifically the local oscillator (LO) frequency changes from 9.75GHz to 10.6GHz.
C Band - LO frequency 9.75GHz
Ku Band - LO frequency 10.6GHz
- Miscellaneous functions based on 22kHz tone PPM encoding, as discussed later in the paper.

Polarization Selection

Polarization is a way to give a transmission signal specific direction. It increases the beam concentration. The signal transmitted by satellite can be polarized in one of four different ways: Linear (horizontal or vertical) or Circular (right-hand or left-hand). Consequently, the satellite can broadcast both H and V or LH and RH polarized signals via one frequency.

The “universal” LNB switches the polarization by looking at the voltage that it receives from the receiver.
12V – Horizontal, 18V – Vertical
13V – Circular right-hand, 20V – Circular left-hand

Generally, only two (12V and 18V or 13V and 20V) will be used with one type of Antenna. Also 1V can be added from a receiver to any of above voltages to compensate for the voltage drop in the co-axial cable, i.e., it could be 13V (12V), 14V (13V), 19V (18V) or 21V (20V) instead.

22kHz Tone and DiSEqC™ (Digital Satellite Equipment Control) Encoding

In addition to selecting the polarization, the LNB needs to select the operating band. This is done with the use of a 22kHz tone frequency. A 22kHz pulse-position modulated signal of about 0.6V amplitude is superimposed on the LNB’s DC power rail. Its coding scheme allows the remote electronics to perform more complex functions like varying the down conversion frequency to select one of multiple LNB’s for dual-dish systems or physically rotating the antenna assembly. Traditionally, when other encoding functions do not require using 22kHz tone, simple presence or absence of this tone selects the operating band by changing the local oscillator frequency of the LNB.

The complex encoding of 22kHz burst is done with a more sophisticated communication bus protocol named DiSEqC standard (Digital Satellite Equipment Control). The open DiSEqC standard developed by the European Telecommunication Satellite Organization is a well accepted worldwide standard for communication between satellite receivers and satellite peripheral equipment.

The 22kHz oscillator has to be a tone generator with specific rise and fall time. The wave shape will be a quasi-square wave. (Sine with flat-top). The required frequency tolerance is ±2kHz over line and temperature variations. Burst coding of this signal is accomplished by input from the microcontroller at the DSQIN pin of the IC as detailed in the datasheet.

22kHz WAVE SHAPE AND DETAILS (See Figures 1 and 2)

Carrier frequency: 22kHz ±2kHz over line and temperature
Carrier amplitude: 650mVpp ±250mV
Modulation mark period: 500µs ±100µs
Modulation space period: 1ms ±200µs

Methods of Modulation

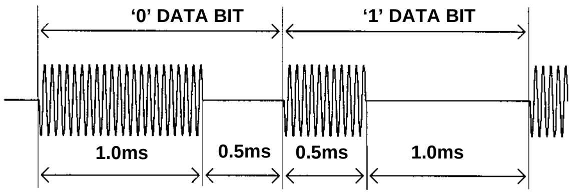


FIGURE 1. DiSEqC™ MODULATION SCHEME

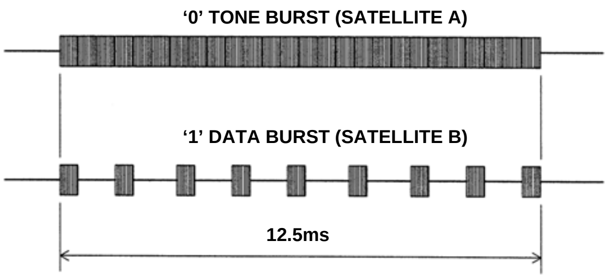


FIGURE 2. TIMING DIAGRAM FOR TONE BURST CONTROL SIGNAL

ISL6405 - Provides a Complete Power Solution for Dual LNB Control

The ISL6405 is a highly integrated solution for supplying power and control signals from advanced satellite set-top box (STB) modules to the low noise blocks (LNBs) of two antenna ports. This dual output device is comprised of two independent current-mode boost PWMs and two low-noise linear regulators along with the circuitry required for I^2C device interfacing and for providing DiSEqC standard control signals to the LNB.

Regulator output voltages are available at two output terminals (VO1, VO2) to support simultaneous operation of two antenna ports in advanced satellite STBs. The regulator outputs for each PWM are set to 13V or 18V by independent voltage select commands (VSEL1, VSEL2) through the I^2C bus. Additionally, to compensate for the voltage drop in the coaxial cable, the selected voltage may be increased by 1V with the line length compensation (LLC) feature. Separate enable commands sent on the I^2C bus provide independent standby mode control for each PWM and linear combination, disabling the output to conserve power.

Both independent tracking current-mode boost converters provide the linear regulators with input voltages that are set to the output voltages, plus typically 1.2V dropout to insure minimum power dissipation across each linear regulator. This maintains constant voltage drops across each linear pass element while permitting adequate voltage range for tone injection.

Please refer to the ISL6405 datasheet, FN9026, for more information.

Quick Start Evaluation

Out Of The Box

The ISL6405 evaluation board is shipped in a "ready-to-test" state. The board requires an input voltage ranging from 8V to 14V and a 3.3V/5V supply. The use of an electronic load enables evaluation over a wide range of operating conditions. The evaluation kit also includes 5 samples of ISL6405EEB and ISL6405ER, a PC to I^2C bus interface board (USB-I2CIO), PC to I^2C bus software, a USB cable, and a connector cable to connect the USB-I2CIO board and the ISL6405EVAL board.

TABLE 1. ISL6405 EVALUATION BOARDS

BOARD NAME	IC	PACKAGE
ISL6405EVAL1C	ISL6405EEB	28-Ld SOIC
ISL6405EVAL2C	ISL6405ER	32-Ld QFN

Required Test Equipment

To fully test the ISL6405 chip functionality, the follow equipment is needed:

- 4 channel oscilloscope with probes
- 2 electronic loads
- 2 bench power supplies
- Precision digital multi-meters
- I^2C bus read/write capability

Power and Load Connections

Refer to the ISL6405EVAL1 and 2 schematics, the reference designators will differ. The ISL6405EVAL1 evaluation board has four sets of terminal posts and three jumpers that are used to supply the input voltages and to monitor and load the outputs.

Jumper and Switch Settings - JP1, JP2, and JP3 will be shorted with shunt jumpers for quick start evaluation. These jumpers can be removed to monitor the input current for each boost regulator or the input bias current of the IC.

The DIP switch, SW1, controls the voltage level at the DSQIN1, DSQIN2, and ADDR pins. The switches are by default in the on position toward the numbers which pull the voltages at these pins to ground.

Input Voltage - Adjust two power supplies to provide the 5V/3.3V and 12V input voltages of the evaluation board. With the power supplies turned off, connect the positive lead of the 12V supply to the VIN post (P1) and the ground lead to the GND post (P2).

The second supply set for either 5V or 3.3V provides the pull-up voltage for the I^2C bus clock and data line. Connect the positive lead of the second supply to the +5V/+3.3V post (P7) and the ground lead to the SGND post (P9).

Output Voltage Loading and Monitoring - To exercise and monitor VOUT1, connect the positive lead of one of the electronic loads and the positive lead of a digital multimeter to the VOUT1 post (P3) and the ground lead to the GND post (P4).

To exercise and monitor VOUT2, connect the positive lead of one of the electronic loads and the positive lead of a digital multimeter to the VOUT2 post (P8) and the ground leads of both to the GND post (P10).

I^2C Bus Communication Setup

To control and exercise the ISL6405 requires communication through the I^2C bus clock (SCL) and data (SDA) pins. Refer to the ISL6405 datasheet for more information about the I^2C bus specification. You can use existing I^2C hardware/software, a word generator, or you the PC to I^2C hardware/software included in the ISL6405 evaluation kit to produce the necessary I^2C waveforms.

USB-I2CIO board driver installation - To use a PC to control the I^2C bus to communicate with the ISL6405 you will have to install the drivers of the USB-I2CIO board included in the kit. You will need a Windows 98/XP/2000 machine with a standard USB port.

1. The evaluation kit comes with a CD containing the software and drivers to control the I^2C bus. Copy the contents of the CD to some directory, e.g., C:\'some directory'.
2. Applying power to the USB-I2CIO board: The USB-I2CIO board has the option of being powered with 3.3V through the USB bus of the PC or externally with 5V connected to the +5 test point and GND test point. The I^2C bus can operate at 3.3V or 5V logic. If you use external 5V then place a shunt jumper shorting pins 2 and 3 of JP3. If you are using an external 5V to power the USB-I2CIO board place a shunt jumper shorting pins 1 and 2 of JP3.
3. After the USB-I2CIO board is powered up, connect the USB cable to the USB port of a PC.
4. Windows should detect the new USB device and the 'Found New Hardware Wizard' should begin. This will help you install the drivers. Follow the directions on the screen until it asks you where to search for the drivers. At this point, you should select the 'choose location' option and browse to the C:\'some directory' created in step one and select the drivers folder.
5. Follow the remaining directions and the driver should be installed and the USB-I2CIO detected by your PC.
6. If this is successful, another 'Found New Hardware Wizard' window will appear. Repeat steps 4 and 5. At this point, the USB-I2CIO board should be ready to use.
7. To connect the USB-I2CIO board to the ISL6405 evaluation board, use the 5-pin to 4-pin connector cable. Connect the 5-pin connector to J4 on the USB-I2CIO board and the 4-pin connector to J3 on the ISL6405 evaluation board. Figure 3 shows the test setup configuration to evaluate the ISL6405 evaluation board.

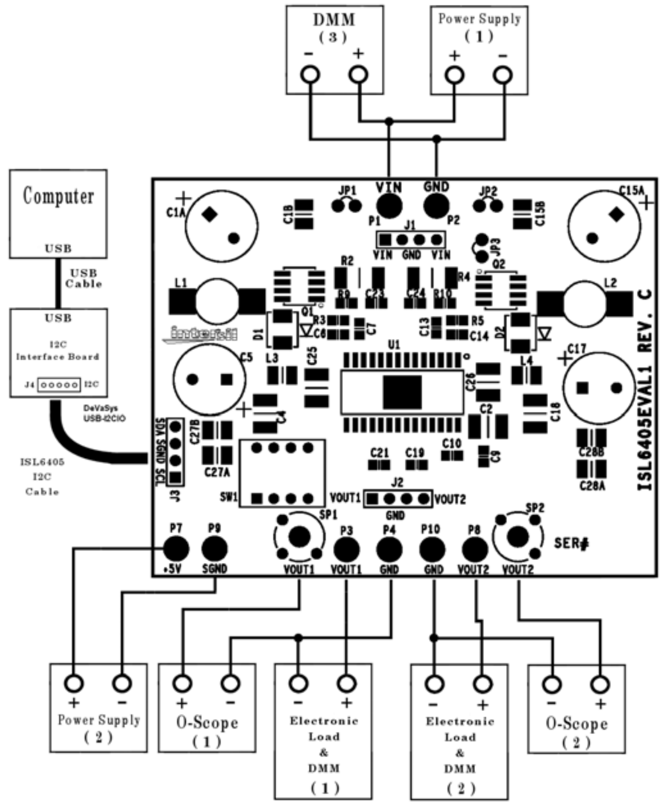


FIGURE 3. ISL6405 TEST SETUP

8. Turn on the power supplies to power up the ISL6405 evaluation board.
9. Run the ISL6405i2crevb.exe program copied to C:\'some directory'. Figure 4 shows the PC to I^2C software application window. Click the 'Open Device' button.
10. If you receive a 'No USB Device Detected' error:
    - Make sure the drivers were installed correctly. If Windows did not detect your USB device, try running the Add/Remove Hardware Wizard in the control panel.
    - Make sure the USB board is powered up (internally or externally, not both).
11. If you receive the 'Incorrect Return Value' error:
    - The ISL6405 evaluation board may not be powered up. Check the power connections.
    - Make sure SCL and SDA are connected correctly. The 5-pin connector to the USB-I2CIO board only fits one way. Try reversing the 4-pin connector at J3 of the ISL6405 evaluation board.

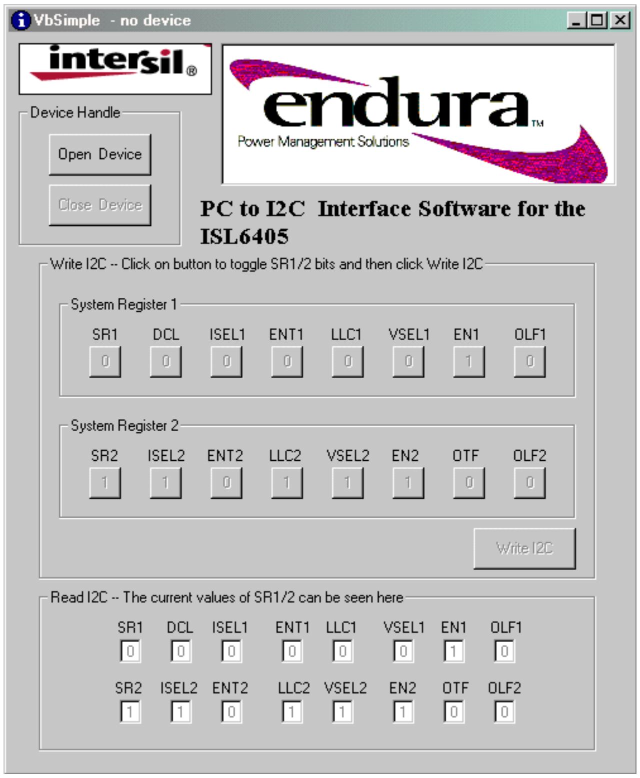


FIGURE 4. PC TO I^{2}C APPLICATION WINDOW

Using the PC to I^{2}C Application

After opening the application window and clicking on the 'Open Device' button, the program will detect the USB-I2CIO board and initialize the I^{2}C system registers of the ISL6405. To evaluate the ISL6405 functionality, toggle the system register bits as needed and then click on the 'Write I2C' button to write to the system registers. The lower portion of the application window shows the current values of the system register bits. They are read and updated continuously. The OLF1/2 and OTF flag in system register 1 and 2 are read only bits and they provide diagnostic status of the ISL6405.

The switch, SW1, allows you to change the I^{2}C address of the ISL6405 by toggling the ADDR pin high or low. With the switch in its default position the ADDR pin is low. The application software will not be able to communicate with the ISL6405 if the ADDR pin is high.

Performance Characterization

Startup

The ISL6405 features internal soft start to reduce external number of components. Figure 5 shows typical soft-start waveform. Typical soft-start time is 4.6ms.

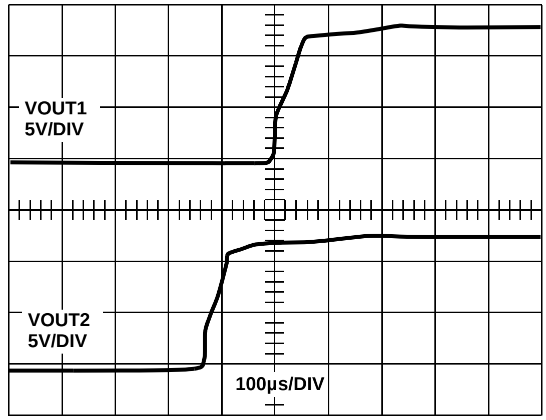


FIGURE 5. SOFT START

Shutdown

Both LNB outputs of ISL6405 can be independently shutdown using ENx bits via I^{2}C. Figure 6 shows typical shutdown waveforms.

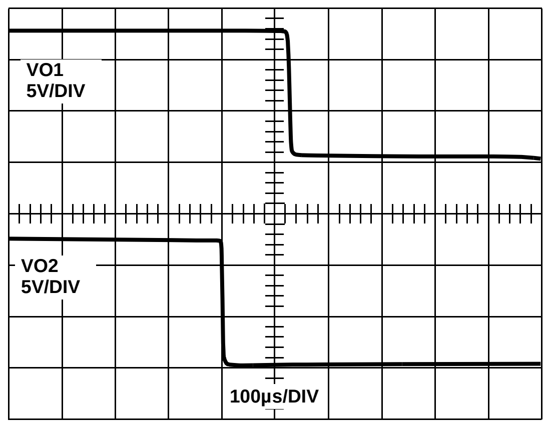


FIGURE 6. SHUTDOWN USING I^{2}C ENABLE

Boost PWM Efficiency

The Boost PWM architecture allows close to 90% efficiency at full load as shown in Figure 7.

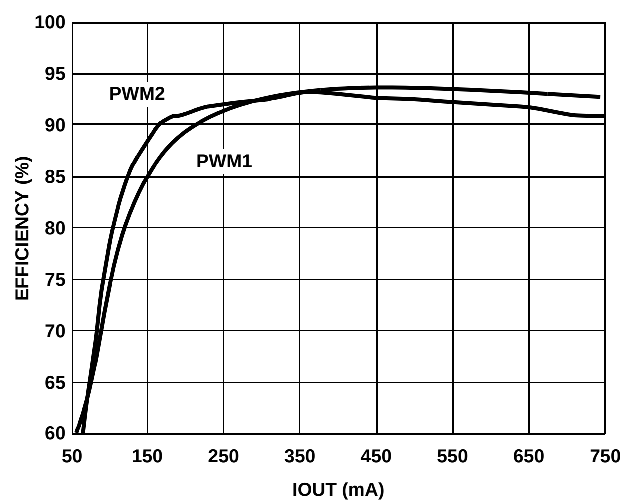


FIGURE 7. BOOST PWM1 AND PWM2 EFFICIENCY vs LOAD

DiSEqC Implementation

The ISL6405 has a built-in 22kHz tone generator that can be controlled either by the I^2C interface or by a dedicated pin (DSQIN) that allows immediate DiSEqC data encoding for the DiSEqC compliance. When the I^2C tone enable bit (ENT) is set to HIGH, a continuous 22kHz tone is generated regardless the status of the DSQIN pin. The ENT pin must be LOW when DSQINx pins are being used for DiSEqC encoding. Figure 8 shows the 22kHz tone waveform with 350mA load.

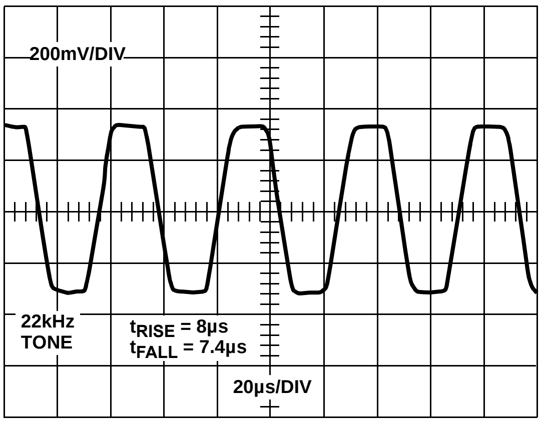


FIGURE 8. 22kHz TONE OPERATION

Overcurrent Hiccup Mode

Figure 9 shows a typical over current trip.

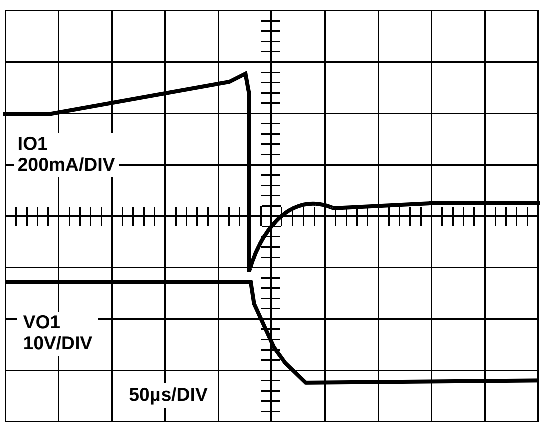


FIGURE 9. OVERCURRENT TRIP

When the DCL (dynamic current limiting) bit is set LOW, the over current protection circuit works dynamically; as soon as an overload is detected, the output is shutdown for a time t_{OFF}, typically 900ms. The output is resumed for a time t_{ON} = 20ms. At the end of t_{ON}, if the overload condition is still detected, the protection circuit will cycle again through t_{OFF} and t_{ON}. Figure 11 shows the typical waveforms for the overcurrent hiccup mode.

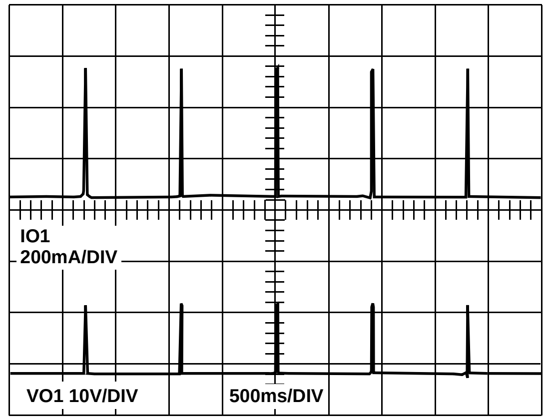


FIGURE 10. OVERCURRENT HICCUP MODE

Output Ripple

Figure 11 shows the typical output ripple waveforms. VO1 is set to 19V and 750mA load. VO2 is set to 13V and 350mA load.

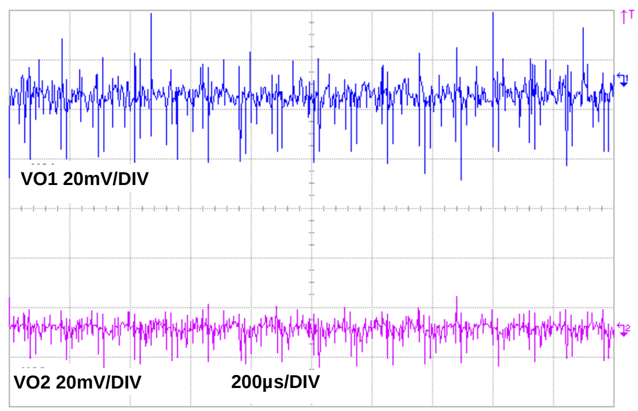


FIGURE 11. OUTPUT RIPPLE

External Back-Bias Protection

Some applications may need to be able to protect the ISL6405 from an inadvertent back-bias voltage condition. For the case where a 24V supply is connected to the output of the ISL6405, a series connected diode as shown in Figure 12 will protect the IC. The LLC bit can be set high through the I^2C bus to increase the output voltage by 1V to compensate for the diode voltage drop.

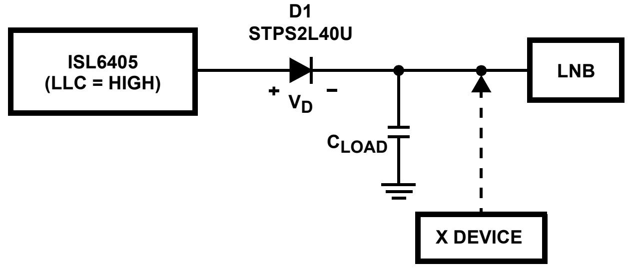


FIGURE 12. DC BACK-BIAS PROTECTION CIRCUIT

The DiSEqC standard recommends a maximum bus load of 0.25µF. For the circuit in Figure 12 to provide proper 22kHz tone operation, the bus would have to have a minimum loading of 12mA.

If tone operation is required at zero load conditions, a resistor can be placed from the cathode of the protection diode to ground, scaled to provide the minimum 12mA. To avoid the added dissipation of this method, a capacitor can be placed in parallel with the back-bias protection diode as shown in Figure 13. This capacitor should be scaled with the capacitive load present on the DiSEqC bus line. For a load of 0.25µF, use a 10µF capacitor. Consider the maximum load of 0.25µF and the highest output voltage of 19V and a 0.5V drop across the Schottky diode. After the tone rise time,

Qd(rise)~0, Qload(rise) = 19V*0.25µF = 4750nC

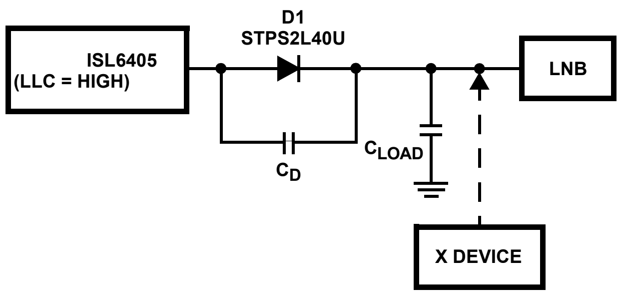


FIGURE 13. DC BACK-BIAS PROTECTION CIRCUIT FOR ZERO LOAD CONDITION

During the tone fall time, the capacitors are essentially in series so the charge will try to equally distribute between Cd and Cload. Cload will discharge allowing current to flow to Cd to match the falling voltage at the anode of the diode. You will have to choose a capacitor, Cd, that is large enough to absorb the Cload discharging current and to minimize the voltage drop created during the minimum tone fall time specification, 5µs. A good choice would be to use a capacitor for Cd that is 4 times the value of Cload.

Figure 14 shows the tone mode operation at the cathode of the protection diode in a zero load condition and the charging current between Cd and Cload. Excessive current transients may occur from a fast dV/dt created if a 24V supply were connected to the output of the ISL6405, therefore, to use the circuit in Figure 13, the 24V supply would have to be limited to 1A maximum current considering the dV/dt voltage transient, to fully protect the IC.

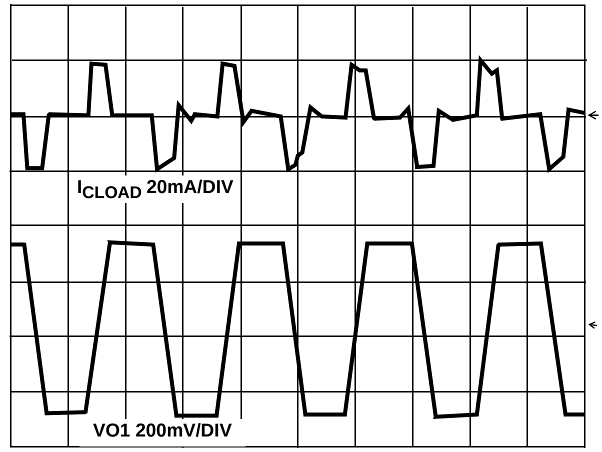


FIGURE 14. ZERO LOAD 22kHz TONE AT CATHODE OF DIODE AND DRIVING CURRENT CHARGING AND DISCHARGING CLOAD

Component Selection Guidelines

The ISL6405EVAL application schematics show the configuration for a dual LNB power supply.

TCAP Capacitor

A capacitor connected to the TCAP pin sets the transition time from 13V to 18V. A minimum 1µF capacitor is required for smooth transition with reduced peak currents. Figure 15 shows the transition time versus capacitor value.

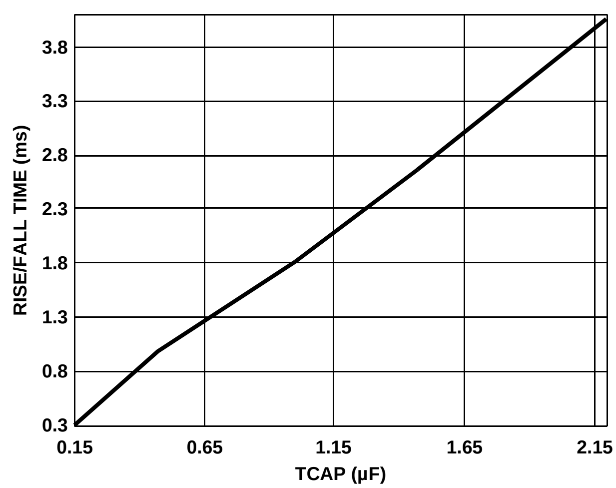


FIGURE 15. TCAP CAPACITOR VALUE vs OUTPUT TRANSITION TIME

The programmed output voltage rise and fall times can be set by an external capacitor. The output rise and fall times will be approximately 3400 times the TCAP value. For the recommended range of 0.47µF to 2.2µF, the rise and fall time would be 1.6ms to 7.6ms. Use of a 0.47µF capacitor insures the PWM will stay below its overcurrent threshold when charging a 120µF VSW filter cap during the worst case 13V to 19V transition. This feature only affects the turn-on and programmed voltage rise and fall times. Figure 16 shows the 13V to 18V transition with TCAP=1uF.

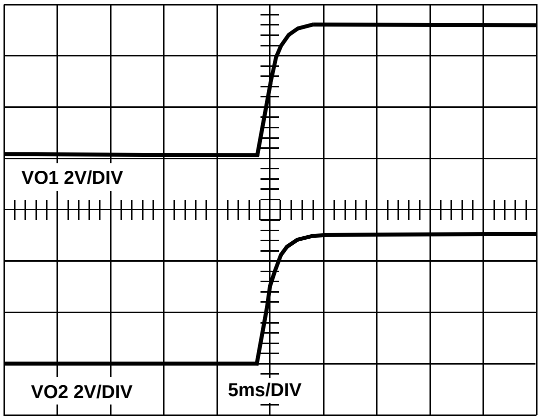


FIGURE 16. 13V TO 18V TRANSITION

Inductor

The ISL6405 operates with a 33µH standard inductor over the entire range of supply voltages and load currents. Choose an inductor that can handle at least the peak switch current without saturating, and ensure that the inductor has a low DCR (series resistance) to maximize efficiency. The inductor saturation current must be greater then the switch peak current,

$$I_{PEAK} = \frac{V_{SW(max)} \cdot I_{OUT}}{N \cdot V_{IN(min)}} + \frac{V_{IN(min)}}{2L \cdot f_{SW}}\left(1 - \frac{V_{IN(min)}}{V_{SW(max)}}\right) \quad \text{(EQ. 1)}$$

where,

L = Inductance 33uH

f_{SW} = PWM switching frequency, 220kHz Typical

N = Efficiency, 92% at maximum load

TABLE 2. RECOMMENDED INDUCTORS

VENDOR	PART NUMBER	ISAT (A)	DCR (mΩ)	PACKAGE
Coilcraft	DS3316P-333	1.4	300	SMD
Toko	A671HN-330L	1.8	21	TH
Coiltronics	DR74-330	1.73	143	SMD

Output Capacitors

The most important parameter for the output capacitors is effective series resistance (ESR). The output ripple is directly proportional to output capacitor ESR value.

A 68µF or less aluminum output filter capacitor with ESR lower than 80mΩ in parallel with a 470nF ceramic capacitor is a good choice in most application conditions. A ceramic capacitor is necessary to reduce the high frequency switching noise.

A high output capacitance and low ESR will strongly reduce the output ripple voltage, output switching noise and improve efficiency. Use the lowest possible ESR capacitor for best performance.

The maximum value output capacitor is restricted by transition time specifications between 13V to 18V. With a high output capacitor the boost circuit will need higher peak current from input supply to make transition from 13V to 18V in an given transition time as set by TCAP value. The Figure 15 shows the TCAP capacitor value versus transition time. Use high TCAP capacitor value for high output capacitors to allow sufficient time to charge the output capacitors in maximum load conditions.

The capacitor's voltage rating should be at least 35V, but higher voltage electrolytic capacitors generally have lower ESR numbers, and for this reason, to improve efficiency and output ripple, select a capacitor with higher voltage ratings.

TABLE 3.

VENDOR	SERIES	PACKAGE
Sanyo	OS-CON Electrolytic	SMD / Through hole
Rubycon		
Nichicon	PL Electrolytic	TH
Panasonic	HFQ Electrolytic	TH
Sprague	594D Electrolytic	SMD

Sense Resistor

The current sense resistor provides current loop feedback and sets over current limit for static current mode. This resistor value is calculated based on peak switch current per Equation 2,

$$R_{SC} < \frac{V_{SENSE}}{I_{PEAK}} \quad \text{(EQ. 2)}$$

Where Vsense is 200mV typ. (see datasheet specification table) and Ipeak is calculated from Equation 1. Make sure the Rsc value is always lower than the Vsense/Ipeak ratio.

In the typical application conditions (VCC = 12V, IOUT (max) = 500mA) a 100mΩ Rsc value is a good choice.

If VIN < 10.5V the inductor peak current can be close to 2A, then, it is necessary to decrease the Rsc value. In the worst case with VIN = 8V, and IOUT = 500mA, low cost axial through-hole resistors could also be used, however, these are usually bigger and need a larger area on the PCB. See Table 4 for some suggested SMD resistor part numbers.

TABLE 4.

VENDOR	SERIES
Meggitt	RL73
SEI Electronics	RMC1
Panasonic	

Layout Guidelines

Just like all switching power supplies, a proper PC board layout is very important for a dual channel ISL6405 based power supply implementation. Protect sensitive analog grounds by using a star ground configuration. Also, minimize lead lengths to reduce stray capacitance, trace resistance, and radiated noise. Minimize ground noise by connecting PGND1/2, the input bypass capacitor ground lead, and the output filter capacitor ground lead to a single point. Place bypass capacitors as close as possible to BYP pin and PGND1/2 and the DC/DC output capacitors as close as possible to VSW1/2.

Place TCAP1/2 capacitors very close to the IC pins and have shortest possible ground return path.

Thermal Design

During normal operation, the ISL6405 dissipates some power. The power dissipation of the output linear regulator dominates the total power dissipated in the ISL6405. At the maximum rated output current, the voltage drop on the linear regulator leads to a total dissipated power that is about 1.2V*750mA*2 = 1.8W. At 350mA maximum current, this power will be 1.2V*350mA*2 = 0.84W. The heat needs to me removed with a heatsink to keep the junction temperature below the over-temperature threshold.

The simplest solution is to use a large, continuous copper area of the ground layer to dissipate the heat. This area can be the inner ground of multi-layered pcbs, or in a dual layer pcb, or an unbroken ground area on the opposite side of the board where the IC is placed. In both cases, the thermal path between the IC ground pins and the dissipating copper area must exhibit a low thermal resistance.

The EPAD SOIC package of the ISL6405 has Rja = 29C/W and Rjc = 4C/W. The QFN package has Rja = 34C/W and Rjc = 6C/W. Due to the presence of exposed pad connected to ground below the IC body on both the EPAD SOIC and the QFN packages, the Rjc is much lower. As a result, a much smaller copper area is required to dissipate heat than standard SOIC packages.

Conclusion

The ISL6405 dual output voltage regulator makes an ideal choice for advanced satellite set-top box and personal video recorder applications. The ISL6405EVAL1 and ISL6405EVAL2 are complete reference designs for providing power and control functions to the LNB in advanced satellite set-top box applications.

References

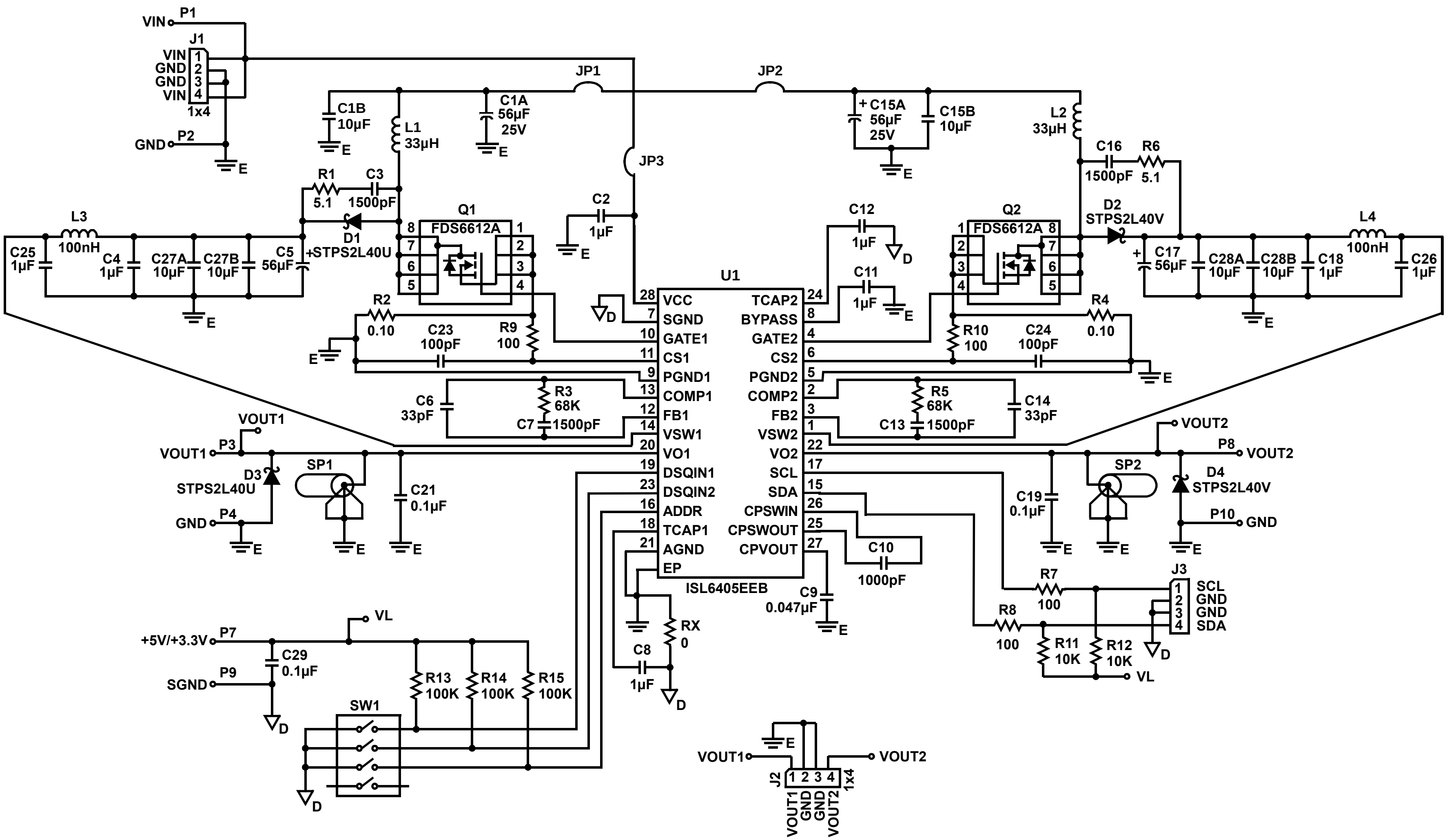
Intersil documents are available on the web at http://www.intersil.com.

[1] *ISL6405 Data Sheet*, Intersil Corporation, File No. FN9026

[2] *DiSEqC Bus Functional Specification*, EUTELSAT http://www.eutelsat.com/docs/diseqc

[3] More information on the USB-I2CIO PC to I^{2}C interface board available at http://www.DeVaSys.com

ISL6405 EVAL1 Schematic



ISL6405 EVAL1 Bill of Materials

REFERENCE	QTY	PART NUMBER	PART TYPE	DESCRIPTION	PACKAGE	VENDOR
U1	1	ISL6405EEB	IC, Linear	Current mode PWM Controller	28LD EPSOIC	Intersil
Q1, Q2	2	FDS6612A	MOSFET Single	N-channel, 30v, 0.022 ohms, 8.4A	SOIC8	Fairchild
D1, D2, D3, D4	4	STPS2L40U	Diode, Schottky, Low Drop Power	Schottky, 30V, 2A	DO-214AA	STMicroelectronics
L1, L2	2	DS3316P-333	Inductor	33uh, 20%, 0.334Ω, 1.4A	DO3316	CoilCraft
L3, L4	2	DN1050CT-ND	Inductor	100nh, 10%, 1175mw	SM_1210	API/Digikey
CAPACITORS						
C1A, C5, C15A, C17	4	25SP56M	Capacitor, Aluminum	56µF, 20%, 25V	CASE-CC	SANYO
C1B, C15B	2	12103G106ZAT2A	Capacitor, Ceramic, Y5V	10µF, 20%, 25v	SM_1210	AVX/Panasonic
C2, C4, C18, C25, C26	5	18125C105MAT2A	Capacitor, Ceramic, X7R	1µF, 20%, 50V	SM_1812	AVX/Panasonic
C3, C16	2	12063C152MAT2A	Capacitor, Ceramic, X7R	1500pF, 20% , 50V	SM_1206	AVX/Panasonic
C6, C14	2	08055A033KAT2A	Capacitor, Ceramic, NPO	33pF, 10%, 50V	SM_0805	AVX/Panasonic
C7, C13	2	08055C152MAT2A	Capacitor, Ceramic, X7R	1500pF, 10% , 50V	SM_0805	AVX/Panasonic
C8, C11, C12	3	0805YC105MAT2A	Capacitor, Ceramic, X7R	1µF, 20%, 16V	SM_0805	AVX/Panasonic
C9	1	08055C473MAT2A	Capacitor, Ceramic, X7R	0.047µF, 20%, 50V	SM_0805	AVX/Panasonic
C10	1	08055C102MAT2A	Capacitor, Ceramic, X7R	1000pF, 20% , 50V	SM_0805	AVX/Panasonic
C19, C21, C29	3	08055C104MAT2A	Capacitor, Ceramic, X7R	0.1µF, 20%, 50V	SM_0805	AVX/Panasonic
C23, C24	2	08055C101MAT2A	Capacitor, Ceramic, X7R	100pF, 20% , 50V	SM_0805	AVX/Panasonic
C27A, C27B, C28A, C28B	4	CE GMK325 F106ZH-T	Capacitor, Ceramic, Y5V	10µFf, 20%, 35v	SM_1210	Taiyo-Yuden
RESISTORS						
R1, R6	2		Resistor, Film	5.1Ω, 5%, 0.25W	SM_1210	Panasonic
R2, R4	2		Resistor, Power metal strip	0.1Ω, 1%, 1W	SM_2512	Panasonic
R3, R5	2		Resistor, Film	68KΩ, 1%, 0.1W	SM_0805	Panasonic
R7, R8, R9, R10	4		Resistor, Film	100Ω, 1%, 0.1W	SM_0805	Panasonic
R11, R12	2		Resistor, Film	10KΩ, 5%, 0.1W	SM_0805	Panasonic
R13, R14, R15	3		Resistor, Film	100KΩ, 5%, 0.1W	SM_0805	Panasonic
Rx - (Do not Populate)	1		Resistor shorted internally	Shorts two grounds paths together.	SM_0805	NA
OTHERS						
SW1	1	78B04S	Switch, Dip	Dip Switch, 4SPST		Grayhill
J1, J2, J3	3	22-03-2041	Connector	Header Strip, 1X4	1X4@.1"	Molex
SP1, SP2	2	TEK131-4353-00	Terminal, Scope Probe	Terminal, Scope Probe		Tektronix
P1-P4, P7-P10	8	1514-2	Turrett Post	Terminal post,through hole,1/4 inch tall	PTH	Keystone
JP1, JP2, JP3	3	68000-236-1X2	Header	1X2 Break Strip GOLD		
JP1, JP2, JP3	3	S9001-ND	Jumper	2 pin jumper		Digikey
	4		Bumpers			

ISL6405EVAL1 Layout

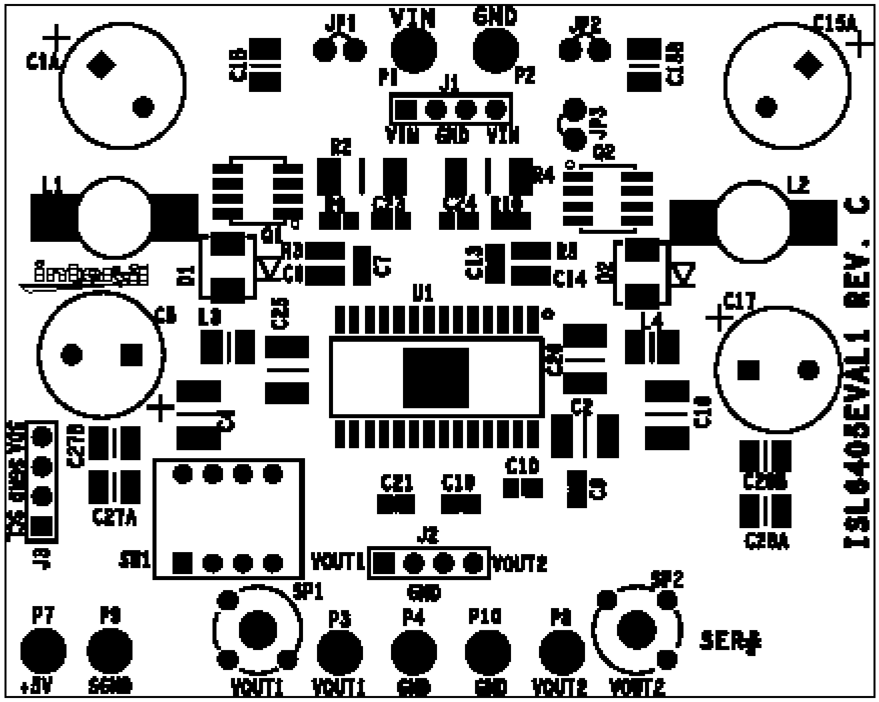


FIGURE 17. TOP SILKSCREEN

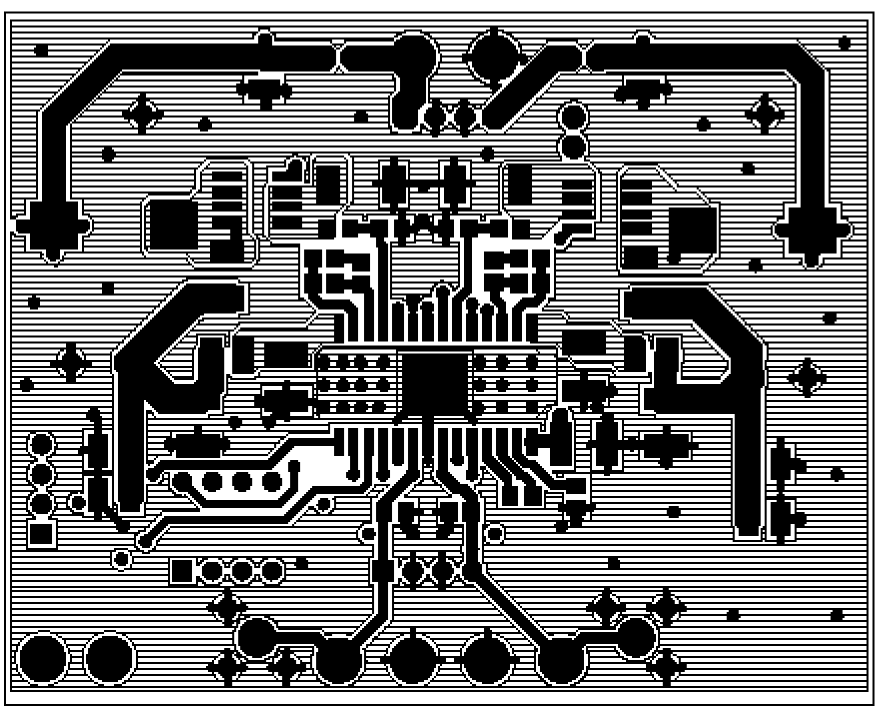


FIGURE 18. LAYER 1

ISL6405EVAL1 Layout (Continued)

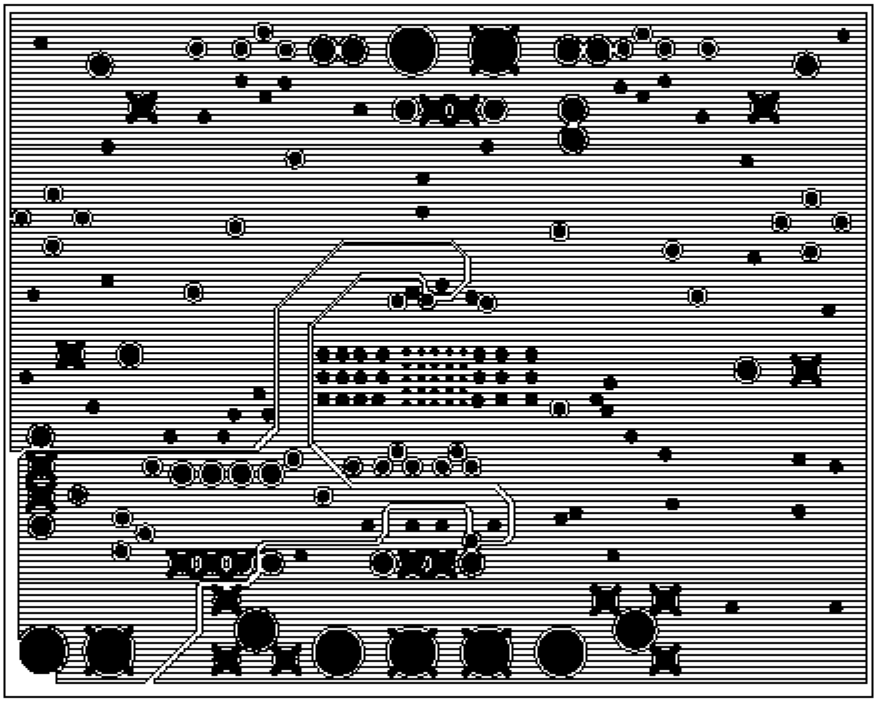


FIGURE 19. LAYER 2

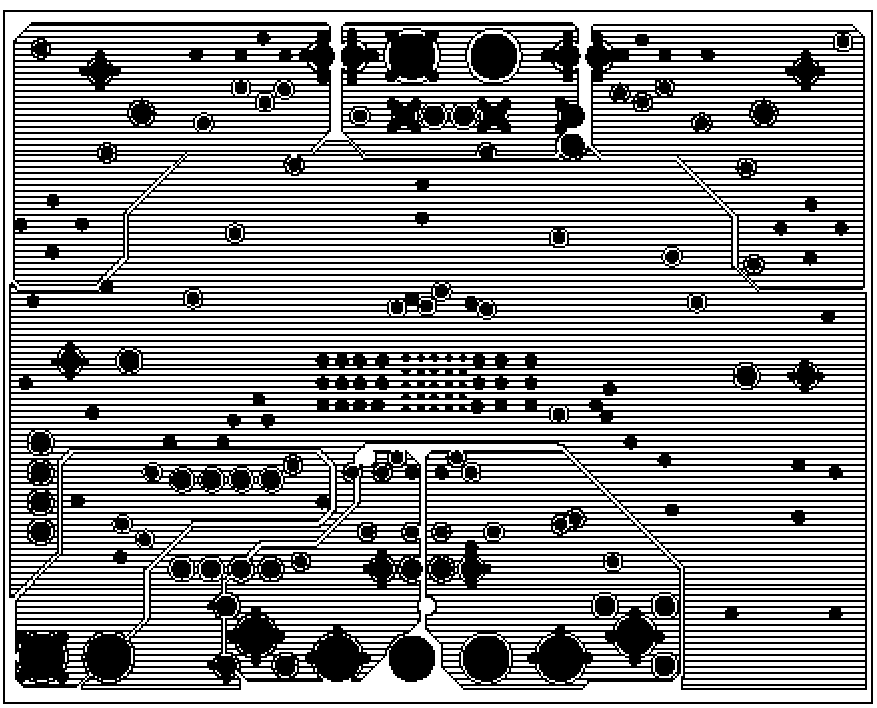


FIGURE 20. LAYER 3

ISL6405EVAL1 Layout (Continued)

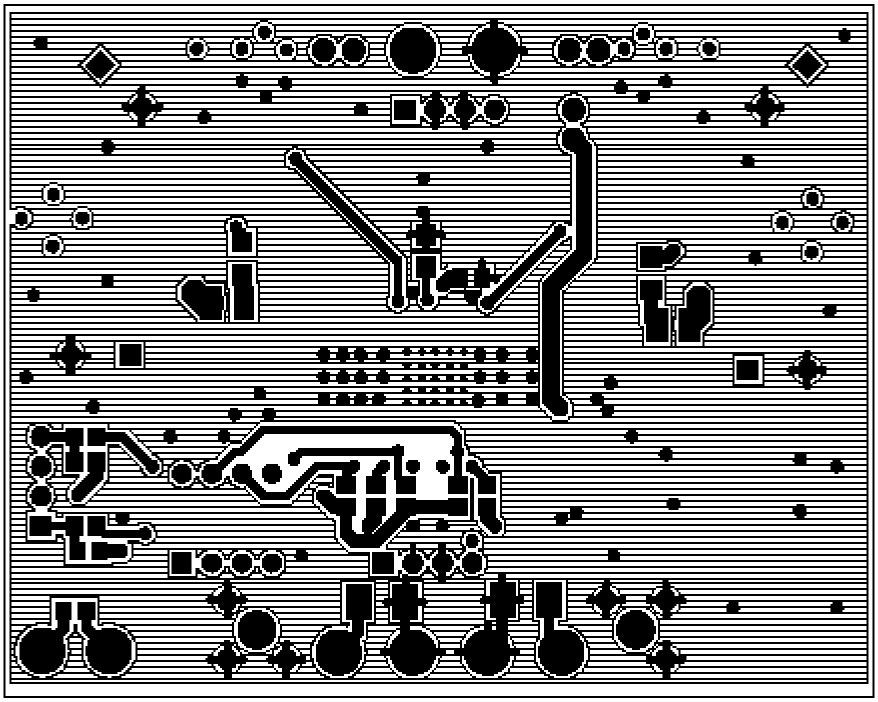


FIGURE 21. LAYER 4

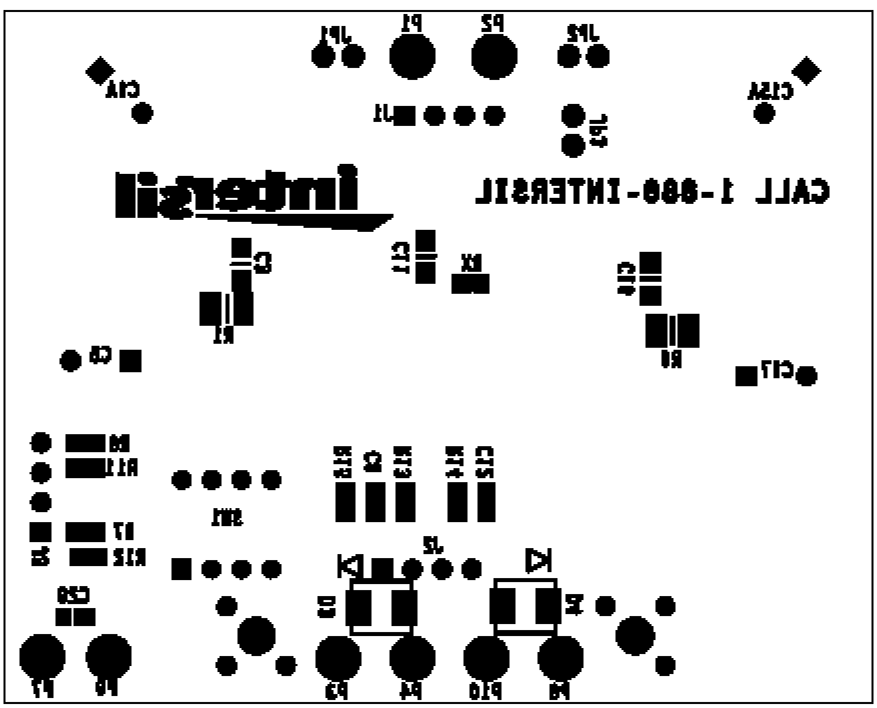
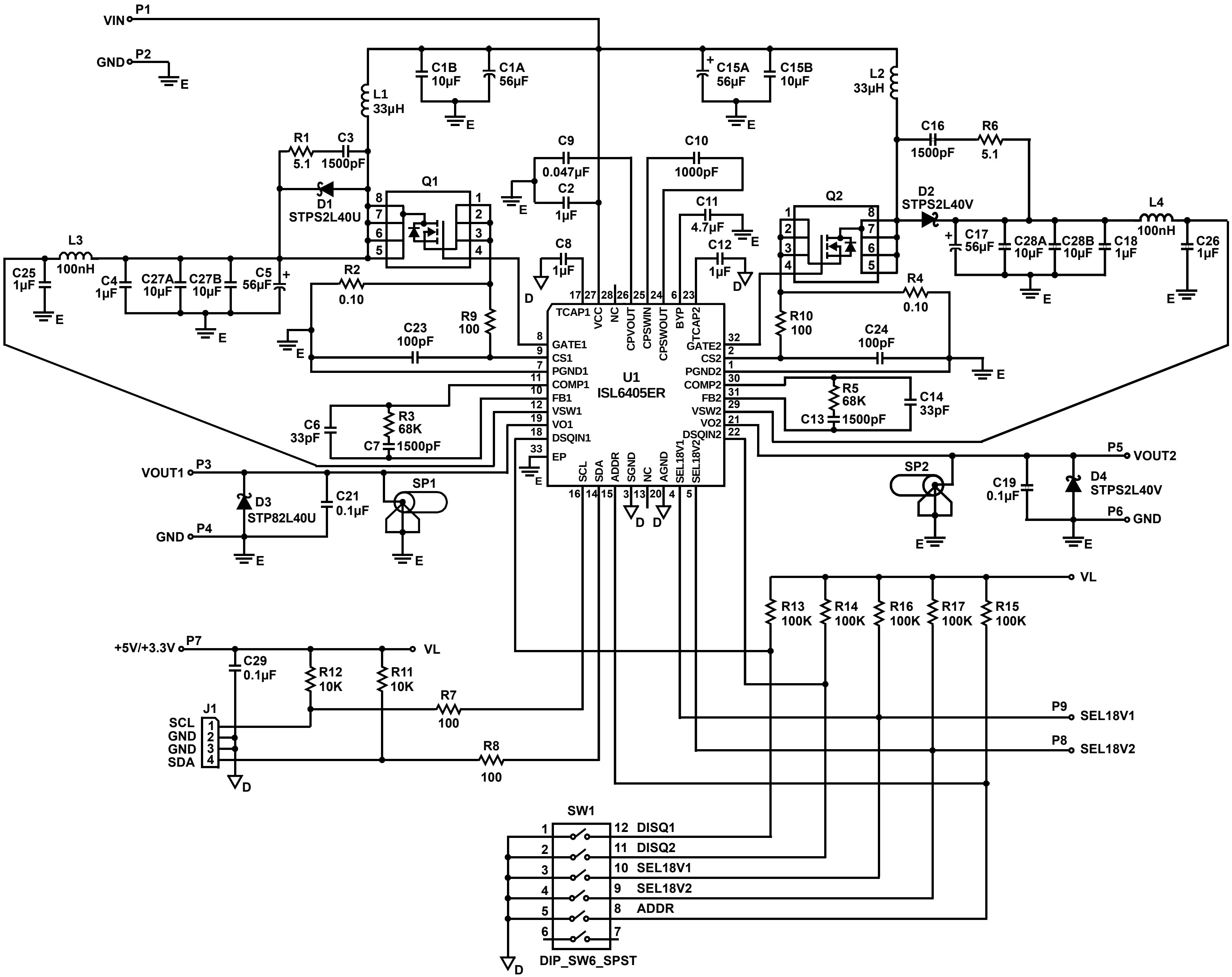


FIGURE 22. BOTTOM SILKSCREEN

ISL6405 EVAL2 Schematic Diagram



ISL6405 EVAL2 Bill of Materials

REFERENCE	QTY	PART NUMBER	PART TYPE	DESCRIPTION	PACKAGE	VENDOR
U1	1	ISL6405ER	IC, Linear	Current mode PWM Controller	32LD QFN (5x5)	Intersil
Q1, Q2	2	FDS6612A	MOSFET Single	N-channel, 30V, 0.022Ω, 8.4A	SOIC8	Fairchild
D1, D2, D3, D4	4	STPS2L40U	Diode, Schottky, Low Drop Power	Schottky, 30V, 2A	DO-214AA	STMicroelectronics
L1, L2	2	DS3316P-333	Inductor	33µH, 20%, 0.334Ω, 1.4A	DO3316	CoilCraft
L3, L4	2	DN1050CT-ND	Inductor	100nH, 10%, 1175mW	SM_1210	API/Digikey
CAPACITORS						
C1A, C5, C15A, C17	4	25SP56M	Capacitor, Aluminum	56µF, 20%, 25V	CASE-CC	SAYNO
C1B, C15B	2	TMK325BJ106M	Capacitor, Ceramic, X5R	10µF, 20%, 25V	SM_1210	Taiyo-Yuden
C2, C4, C18, C25, C26, C8, C12	7	12105C105MAT2A	Capacitor, Ceramic, X7R	1µF, 20%, 50V	SM_1210	AVX/Panasonic
C6, C14	2	08055A033KAT2A	Capacitor, Ceramic, NPO	33pF, 10%, 50V	SM_0805	AVX/Panasonic
C3, C7, C13, C16	4	08055C152MAT2A	Capacitor, Ceramic, X7R	1500pF, 10% , 50V	SM_0805	AVX/Panasonic
C19, C21, C29	3	08055C104MAT2A	Capacitor, Ceramic, X7R	0.1µF, 20%, 50V	SM_0805	AVX/Panasonic
C9	1	08055C473MAT2A	Capacitor, Ceramic, X7R	0.047µF, 20%, 50V	SM_0805	AVX/Panasonic
C10	1	08055C102MAT2A	Capacitor, Ceramic, X7R	1000pF, 10% , 50V	SM_0805	AVX/Panasonic
C23, C24	2	08055C101MAT2A	Capacitor, Ceramic, X7R	100pF, 20% , 50V	SM_0805	AVX/Panasonic
C11	1	1210YC475MAT2A	Capacitor, Ceramic, X7R	4.7µF, 20%, 16V	SM_1210	AVX/Panasonic
C27A, C27B, C28A, C28B	4	GMK325 F106ZH-T	Capacitor, Ceramic, Y5V	10µF, +80-20%, 35V	SM_1210	Taiyo-Yuden
RESISTORS						
R1, R6	2		Resistor, Film	5.1Ω, 5%, 0.1W	SM_0805	Panasonic
R2, R4	2		Resistor, Power metal strip	0.1Ω, 1%, 1W	SM_2512	Panasonic
R3, R5	2		Resistor, Film	68KΩ, 1%, 0.1W	SM_0805	Panasonic
R7, R8, R9, R10	4		Resistor, Film	100Ω, 1%, 0.1W	SM_0805	Panasonic
R11, R12	2		Resistor, Film	10KΩ, 5%, 0.1W	SM_0805	Panasonic
R13, R14, R15, R16, R17	5		Resistor, Film	100KΩ, 5%, 0.1W	SM_0805	Panasonic
OTHERS						
SW1	1	78B06S	Switch, Dip	Dip Switch, 6SPST		Grayhill
J1	1	22-03-2041	Connector	Header Strip, 1X4	1X4@.1"	Molex
SP1, SP2	2	129 0701 202	Terminal, Scope Probe	Terminal, Scope Probe		Johnson
P1 - P9	9	1514-2	Turrett Post	Terminal post,through hole,1/4 inch tall	PTH	Keystone
	4		Bumpers			

ISL6405EVAL2 Layout

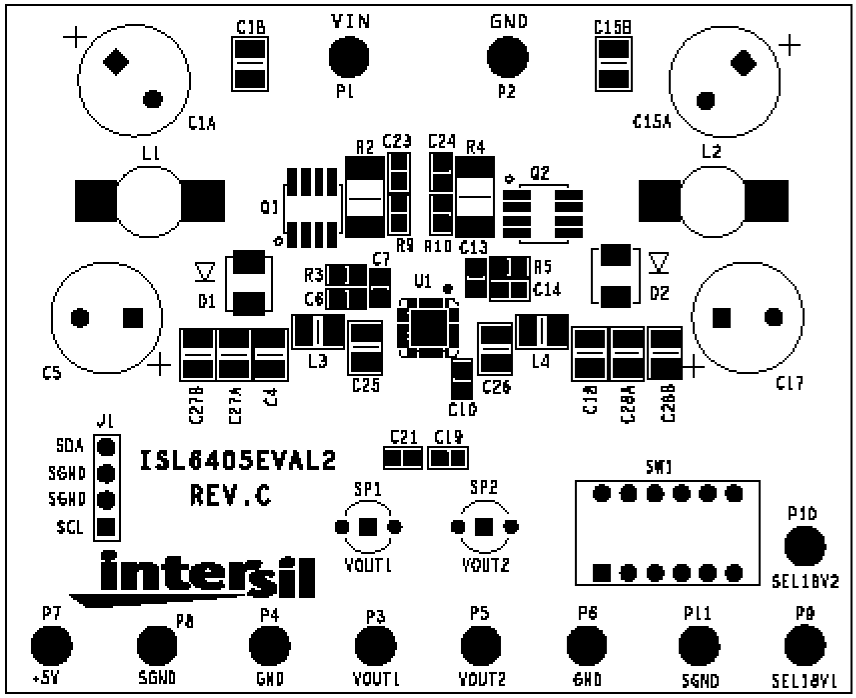


FIGURE 23. TOP SILKSCREEN

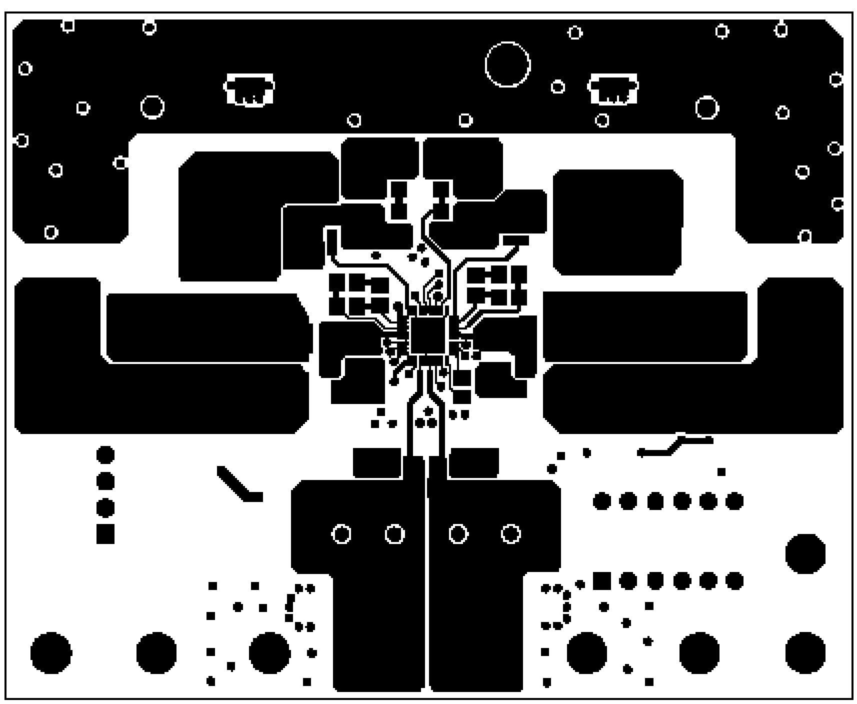


FIGURE 24. LAYER 1

ISL6405EVAL2 Layout (Continued)

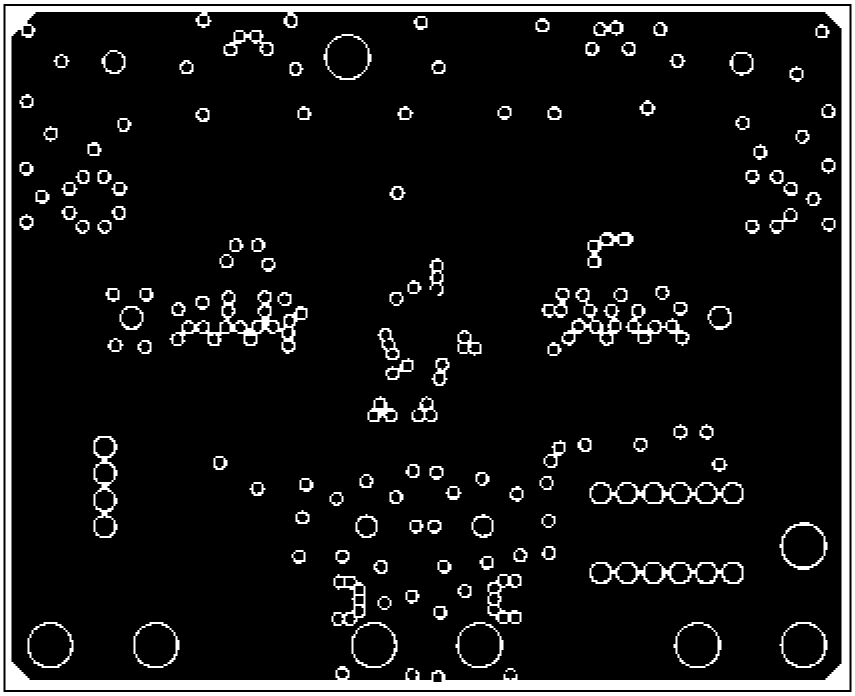


FIGURE 25. LAYER 2

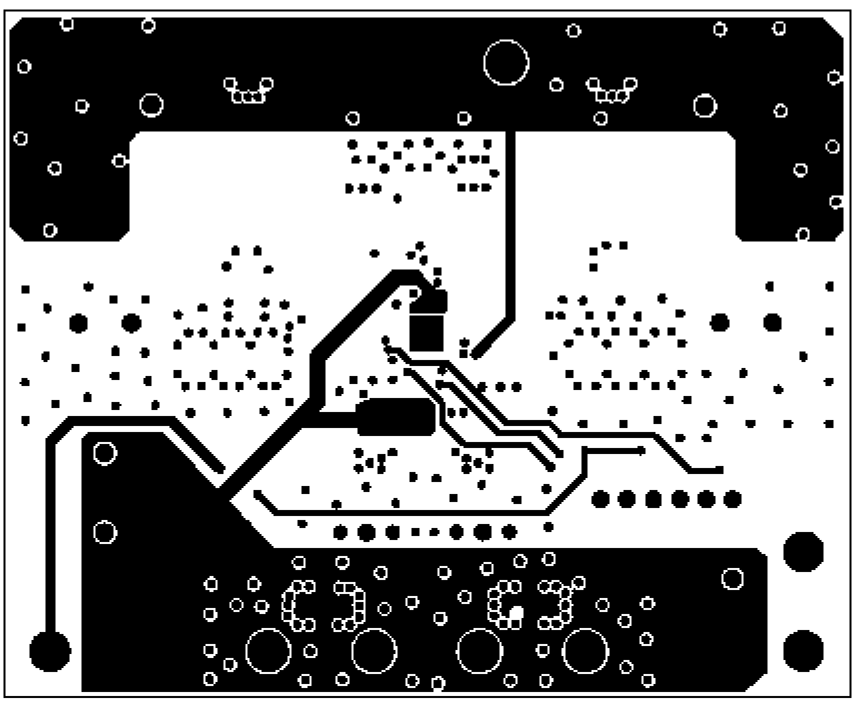


FIGURE 26. LAYER 3

ISL6405EVAL2 Layout (Continued)

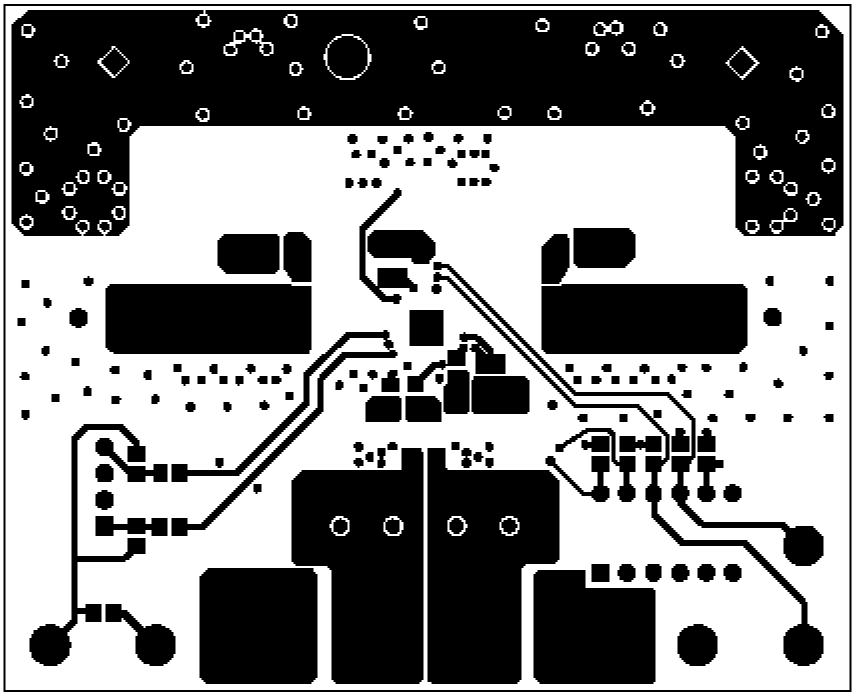


FIGURE 27. LAYER 4

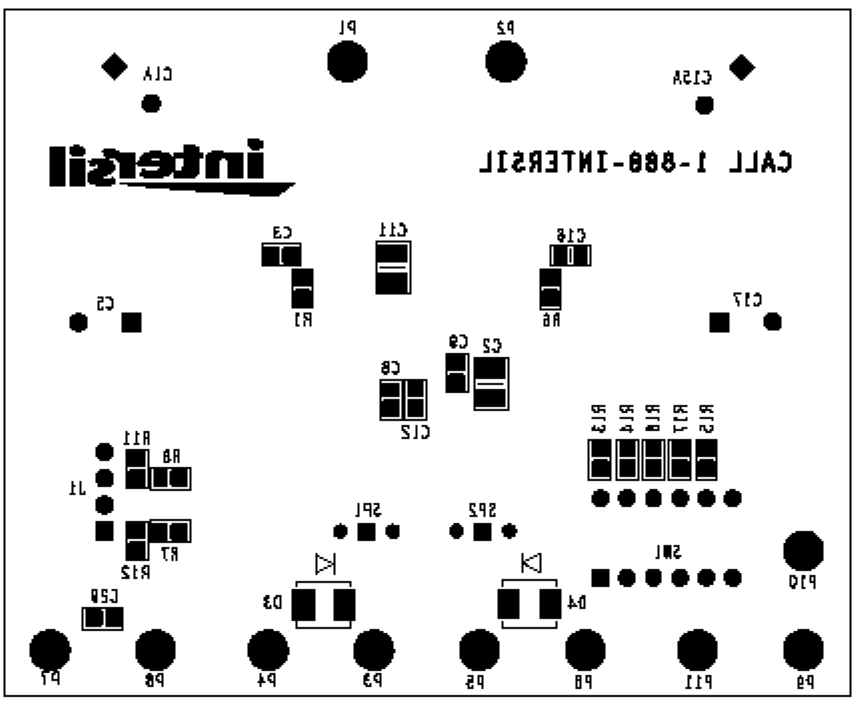


FIGURE 28. BOTTOM SILKSCREEN

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